CLAIMS

What is claimed is:

1. A printing stencil adapted for registration with an electronic substrate about a locus, the stencil comprising a stencil body and an array of printing orifices passing through the stencil body, the printing orifices having varying sizes, with the size of each printing orifice being a function of a distance of the printing orifice from the locus.

2. The printing stencil of claim 1 wherein the size of each printing orifice is linearly correlated to the distance of the printing orifice from the locus.

3. The printing stencil of claim 1 further comprising at least one non-printing orifice in the stencil body.

4. The printing stencil of claim 3 wherein the non-printing orifice comprises a registration hole for receiving a registration pin.

5. The printing stencil of claim 1 wherein the stencil body comprises a metal foil.

6. The printing stencil of claim 1 wherein the locus comprises a center of the stencil body.

7. The printing stencil of claim 1 wherein the locus comprises a location equidistant from a plurality of fiducial alignment locations adapted for alignment with corresponding fiducial marks carried on a substrate.

8. The printing stencil of claim 1 wherein the size of each printing orifice is a first size adjusted by a size scaling factor, the size scaling factor being equal to one at the locus and increasing radially outwardly therefrom.

9. The printing stencil of claim 8 wherein the size scaling factor increases linearly outwardly from the locus.

10. The printing stencil of claim 8 wherein the size scaling factor increases non-linearly outwardly from the locus.

11. The printing stencil of claim 8 wherein the size scaling factor decreases outwardly from the locus.

12. The printing stencil of claim 1 wherein the size of each printing orifice may be calculated according to the formula $S=S_0(1+n_xd_x)$, wherein S is the size of the orifice, S_0 is an initial printing orifice size, n_x is a directional size scaling constant related to a first direction x, and d_x is the distance measured in the first direction x of the printing orifice from the locus.

13. The printing stencil of claim 1 wherein the size of each printing orifice may be calculated according to the formula $S=S_0(1 + n_xd_x + n_yd_y)$, wherein S is the size of the orifice, S_0 is an initial printing orifice size, n_x is a first directional size scaling constant related to a first direction x, n_y is a second directional size scaling constant related to a second direction y, d_x is the distance measured in the first direction x of the printing orifice from the locus and d_y is the distance measured in the second direction y of the printing orifice from the locus.

14. A printing stencil adapted for registration with an electronic substrate about a locus, the stencil comprising a stencil body, a first component set of printing orifices passing through the stencil body proximate the locus, and a second component set of printing orifices passing through the stencil body, the printing orifices of the first component set having a first size and being configured to correspond to a configuration of contacts on a single component type that is to be surface mounted to a board, the printing orifices of the second component set having a second size different from the first size and being configured to correspond to a configuration of contacts of the same single component type.

15. The printing stencil of claim 14 wherein each of the first and second component sets comprises a pair of printing orifices, one printing orifice of the pair being positioned for alignment with a first contact of one component and the other printing orifice of the pair being positioned for alignment with a second contact of the same component.

16. The printing stencil of claim 14 further comprising at least one non-printing orifice in the stencil body.

17. The printing stencil of claim 14 wherein the locus comprises a center of the stencil body.

18. The printing stencil of claim 14 wherein the locus comprises a location equidistant from a plurality of fiducial alignment locations adapted for alignment with corresponding fiducial marks carried on a substrate.

19. The printing stencil of claim 14 the second size is equal to the first size adjusted by a size scaling factor, the size scaling factor being proportional to a distance of the second component set from the locus.

20. A soldering stencil adapted for applying solder to terminals of a terminal array carried by an electronic substrate, the stencil comprising a stencil body having a center and an array of solder orifices passing through the stencil body, at least one central solder orifice of the array having a first size, other solder orifices of the array having a size differing from the first size, with the change in the size of the other solder orifices being determined by a size scaling factorwhich is proportional to a distance of the solder orifice from the center of the stencil body.

21. The printing stencil of claim 20 wherein the size scaling factor changes linearly outwardly from the locus.

22. The printing stencil of claim 21 wherein the size scaling factor increases linearly outwardly from the locus.

23. The printing stencil of claim 20 wherein the size scaling factor for each orifice is equal to $1+n_xd_x+n_yd_y$, wherein n_x is a first directional size scaling constant related to a first direction x, n_y is a second directional size scaling constant related to a second direction y, d_x is the distance measured in the first direction x of the printing orifice from the locus and d_y is the distance measured in the second direction y of the printing orifice from the locus.

24. The printing stencil of claim 23 wherein the substrate changes dimensions anisitropically during processing and n_x is different from n_y.

25. The printing stencil of claim 23 wherein $n_y=0$.

26. The printing stencil of claim 20 further comprising at least one non-printing orifice in the stencil body.

27. The printing stencil of claim 26 wherein the non-printing orifice comprises a registration hole for receiving a registration pin.

28. The printing stencil of claim 20 wherein the stencil body comprises a metal foil.

29. The printing stencil of claim 20 wherein the terminals of the substrate are initially applied in an initial array and the substrate is dimensionally altered to reposition the terminals in the terminal array, each of the solder orifices of the stencil being displaced by a predetermined offset from a position corresponding to a position of an associated terminal in the initial array, the offset for each solder orifice being proportional to a distance of the solder orifice from the center of the stencil body.

30. A printing stencil adapted for registration with an electronic substrate, the electronic substrate bearing an array of terminals, the terminals in the array having an initial relative orientation in an initial terminal array, the stencil comprising:

a stencil body and an array of printing orifices passing through a thickness of the stencil body, each of the printing orifices being displaced by a predetermined offset from a center of the stencil body, the offset for each printing orifice being proportional to a distance of the printing orifice from the center.

31. The printing stencil of claim 30 further comprising at least one non-printing orifice in the stencil body.

32. The printing stencil of claim 31 wherein the non-printing orifice comprises a registration hole for receiving a registration pin.

33. The printing stencil of claim 30 wherein the stencil body comprises a metal foil.

34. The printing stencil of claim 30 wherein the locus comprises a center of the stencil body.

35. The printing stencil of claim 30 wherein a central one of the printing orifices encompasses the center of the stencil body, the predetermined offset for the central printing orifice being zero, whereby the position of the central orifice corresponds directly to the position of a corresponding central target in the initial target array.

36. The printing stencil of claim 30 wherein the printing orifices have varying sizes, with the size of each printing orifice being correlated to the distance of the printing orifice from the center.

37. A printing stencil for use with a substrate which carries a plurality of terminals having a predetermined size, the terminals being initially arranged on the substrate in an initial terminal array, the stencil comprising:

a stencil body, a locus, and plurality of printing orifices in the stencil body, the size of each printing orifice being correlated to a first size by a size scaling factor and the position of each printing orifice being displaced by a

predetermined offset from a position corresponding to a position of an associated terminal in the initial terminal array, the size scaling factor and the magnitude of the predetermined offset for each printing orifice being proportional to a distance of the printing orifice from the locus.

38. The printing stencil of claim 37 wherein the size scaling factor and the magnitude of the predetermined offset are each linearly proportional to the distance of the printing orifice from the locus.

39. The printing stencil of claim 37 wherein the size scaling factor changes linearly with the distance from the locus.

40. The printing stencil of claim 37 wherein the size scaling factor increases linearly with the distance from the locus.

41. The printing stencil of claim 37 wherein the size scaling factor increases non-linearly with the distance from the locus.

42. The printing stencil of claim 37 wherein the size scaling factor is one at the locus, such that an orifice centered about the locus has the first size, and the size scaling factor changes linearly with the distance from the locus.

43. The printing stencil of claim 42 wherein the size scaling factor increases linearly with the distance from the locus.

44. The printing stencil of claim 37 wherein the magnitude of the predetermined offset increases linearly with the distance from the locus.

45. A subassembly for manufacturing an electronic device, comprising:

an electronic substrate having a first surface, a substrate locus, circuitry, and a plurality of terminals carried on the first surface and electrically coupled to the circuitry, the terminals having moved with respect to one another from an initial terminal array in which the terminals had a first relative position to a stenciling array in which the targets have a second relative position; and

a stencil having a second surface, a stencil locus, and a plurality of solder orifices extending through a thickness of the stencil, each of the solder orifices being displaced by a predetermined offset from a position corresponding to a position of an associated terminal in the initial terminal array, the offset for each solder orifice being proportional to a distance of the solder orifice from the stencil locus;

the second surface of the stencil being juxtaposed with the first surface of the substrate, the stencil locus being registered with the substrate locus.

46. The subassembly of claim 45 further comprising at least one non-printing orifice in the stencil body.

47. The subassembly of claim 45 wherein the stencil comprises a metal foil.

48. The subassembly of claim 45 wherein the stencil locus comprises a center of the stencil body.

49. The subassembly of claim 48 wherein a central one of the printing orifices is centered on the center of the stencil body, the predetermined offset for the central printing orifice being zero, whereby the position of the central orifice corresponds directly to the position of a corresponding central target in the initial target array.

50. The subassembly of claim 45 wherein the substrate locus comprises a location equidistant from a plurality of fiducial marks carried by the substrate.

51. A method of applying solder paste on an electronic substrate using a stencil, comprising:

providing an electronic substrate comprising a substrate body and a plurality of terminals, the substrate body having circuitry, a first surface and a substrate locus, the terminals being electrically coupled to the circuitry and being carried on the first surface in an altered relative relationship which differs from an initial relative relationship in an initial terminal array;

providing a stencil having a stencil body, a second surface, a stencil locus, and a plurality of solder orifices passing through the stencil body, each solder orifice having a size correlated to an ideal size by a size scaling factor and the position of each solder orifice being displaced by a predetermined offset from a position corresponding to a position of an associated terminal in the initial terminal array, the size scaling factor and the position scaling factor being proportional to a distance from the stencil locus;

juxtaposing the first and second surfaces with the stencil locus in registry with the substrate locus; and

passing a solder paste through the solder orifices to deposit a discrete volume of solder paste on each corresponding terminal.

52. The method of claim 51 wherein the volume of solder delivered through each of the solder orifices is proportional to the size of the orifice, the volume of solder paste delivered through orifices closer to the stencil locus

being less than the volume of solder paste delivered through orifices farther from the stencil locus.

53. The method of claim 51 wherein the stencil further comprises an outer face oriented away from the substrate, the solder being passed through the solder orifices by drawing a squeegee across the outer face of the stencil, the size of each orifice and a thickness of the stencil body determining the volume of solder paste delivered through the orifice.

54. A method of applying solder paste on an electronic substrate using a stencil, comprising:

providing an electronic substrate comprising a substrate body and a plurality of terminals, the substrate body having circuitry, a first surface and a substrate locus, the terminals being electrically coupled to the circuitry and being carried on the first surface in a predetermined relative relationship to define an initial terminal array;

dimensionally altering the substrate body such that the relative relationship of the terminals differs from the predetermined relative relationship;

providing a stencil having a stencil body, a second surface, a stencil locus, and a plurality of solder orifices passing through the stencil body, each solder orifice having a size correlated to an ideal size by a size scaling factor and the position of each solder orifice being displaced by a predetermined offset from a position corresponding to a position of an associated terminal in the initial terminal array, the size scaling factor and the position scaling factor being proportional to a distance from the stencil locus;

juxtaposing the first and second surfaces with the stencil locus in registry with the substrate locus; and

passing a solder paste through the solder orifices to deposit a discrete volume of solder paste on each corresponding terminal.

55. A method of designing a stencil for applying solder paste on an electronic substrate, comprising:

determining initial positions of a plurality of electrically conductive terminals in an initial terminal array to be carried by the substrate;

estimating a size scaling constant to reflect changes in positions of the terminals from their initial positions in light of anticipated handling of the substrate prior to solder deposition;

identifying a stencil locus of the stencil;

arranging a plurality of solder orifices, with a separate solder orifice corresponding to each terminal;

selecting an initial solder orifice size to deliver an appropriate volume of solder paste to an underlying terminal; and

sizing each solder orifice by multiplying the initial solder orifice size by a size scaling factor proportional to the size scaling constant, the size scaling factor being 1 at the stencil locus and changing outwardly therefrom in proportion to a distance of the solder orifice from the stencil locus.

56. The method of claim 55 wherein the size scaling constant is estimated by handling a plurality of electronic substrates similar to the substrates with which the stencil will be used according to the anticipated handling and measuring variations in positions of the terminals from their initial positions.

57. The method of claim 55 wherein the size scaling factor is estimated based on known behavior of the material of which the substrate is formed.

58. The method of claim 55 wherein a center of the stencil is identified as the stencil locus.

59. The method of claim 55 wherein the size of each orifice may be calculated according to the formula $S=S_0(1+nd)$, wherein S is the size of the orifice, S_0 is the initial solder orifice size, n is the size scaling constant and d is the distance of the solder orifice from the stencil locus.

60. The method of claim 55 wherein the size of each orifice is equal to a size S determined according to the formula $S=S_0(1+n_xd_x)$, wherein S_0 is an initial printing orifice size, n_x is a directional size scaling constant related to a first direction x, and d_x is the distance measured in the first direction x of the printing orifice from the locus.

61. The method of claim 55 wherein the size of each orifice is equal to a size S determined according to the formula $S=S_0(1+n_xd_x+n_yd_y)$, wherein S_0 is an initial printing orifice size, n_x is a first directional size scaling constant related to a first direction x, n_y is a second directional size scaling constant related to a second direction y, d_x is the distance measured in the first direction x of the printing orifice from the locus and d_y is the distance measured in the second direction y of the printing orifice from the locus.

62. A method of designing a stencil for applying solder paste on a plurality of like electronic substrates, comprising:

determining initial positions of a plurality of electrically conductive terminals in an initial terminal array to be carried by the substrates;

determining a position scaling constant and a size scaling constant to reflect changes in positions of the terminals from their initial positions in light of anticipated handling of the substrates prior to solder deposition;

identifying a stencil locus of the stencil;

arranging a plurality of solder orifices for the stencil, with a separate solder orifice corresponding to each terminal, by displacing each solder orifice from an ideal position by a predetermined offset correlated to the position scaling constant, the ideal position for each solder orifice corresponding to a position of an associated target in the initial target array, the offset for each solder orifice being proportional to a distance of the ideal position of the solder orifice from the stencil locus;

selecting an initial solder orifice size to deliver an appropriate volume of solder paste to an underlying terminal; and

sizing each solder orifice by multiplying the initial solder orifice size by a size scaling factor proportional to the size scaling constant, the size scaling factor being 1 at the stencil locus and changing outwardly therefrom in proportion to a distance of the orifice from the stencil locus.

63. The method of claim 62 wherein the size scaling constant is estimated by handling a plurality of electronic substrates similar to the substrates with which the stencil will be used according to the anticipated handling and measuring variations in positions of the terminals from their initial positions.

64. The method of claim 62 wherein the size scaling factor is estimated based on known behavior of the material of which the substrate is formed.

65. The method of claim 62 wherein a center of the stencil is identified as the stencil locus.

66. The method of claim 62 wherein the size of each orifice is equal to a size S determined according to the formula $S=S_0(1+nd)$, wherein S_0 is the initial solder orifice size, n is the size scaling constant and d is the distance of the solder orifice from the stencil locus.

67. The method of claim 66 wherein the position of each orifice is equal to a position P determined according to the formula $P=P_0 + md$, wherein P_0 is the ideal position of the orifice, m is the position scaling constant, and *d* is a vector extending from the stencil locus to P_0.

68. The method of claim 62 wherein the size of each orifice is equal to a size S determined according to the formula $S=S_0(1 + n_xd_x + n_yd_y)$, wherein S_0 is an initial printing orifice size, n_x is a first directional size scaling constant related to a first direction x, n_y is a second directional size scaling constant related to a second direction y, d_x is the distance measured in the first direction x of the printing orifice from the locus and d_y is the distance measured in the second direction y of the printing orifice from the locus.

69. The method of claim 68 wherein $n_y=0$.

70. The method of claim 62 wherein the position of each orifice is equal to a position P determined according to the formula $P=P_0 + md$, wherein P_0 is the ideal position of the orifice, m is the position scaling constant, and *d* is a vector extending from the stencil locus to P_0.

71. The method of claim 62 wherein the position of each orifice is equal to a position P determined according to the formula $P=P_0 + m_xd_x + m_yd_y$, wherein P_0 is the ideal position of the orifice, m_x is a first directional position scaling constant related to a first direction x, m_y is a second

directional position scaling constant related to a second direction y, d is a vector extending from the stencil locus to P_0, d_x is a first vector component of the vector d along the first direction x, and d_y is a second vector component of the vector d along the second direction y.

72. A computer readable storage medium containing a computer readable code for operating a computer to perform a method of designing a stencil for applying solder paste on an electronic substrate, the method comprising:

determining initial positions of a plurality of electrically conductive terminals in an initial terminal array to be carried by the substrates;

estimating a size scaling constant to reflect changes in positions of the terminals from their initial positions in light of anticipated handling of the substrates prior to solder deposition;

identifying a stencil locus of the stencil;

arranging a plurality of solder orifices for the stencil, with a separate solder orifice corresponding to each terminal;

selecting an initial solder orifice size to deliver an appropriate volume of solder paste to an underlying terminal; and

sizing each solder orifice by multiplying the initial solder orifice size by a size scaling factor proportional to the size scaling constant, the size scaling factor being 1 at the stencil locus and changing outwardly therefrom in proportion to a distance of the solder orifice from the stencil locus.

73. The storage medium of claim 72 wherein the size scaling constant is estimated by handling a plurality of electronic substrates similar to the substrates with which the stencil will be used according to the anticipated

handling and measuring variations in positions of the terminals from their initial positions.

74. The storage medium of claim 72 wherein the size scaling factor is estimated based on known behavior of the material of which the substrate is formed.

75. The storage medium of claim 72 wherein a center of the stencil is identified as the stencil locus.

76. The storage medium of claim 72 wherein the size of each orifice may be calculated according to the formula $S=S_0(1+nd)$, wherein S is the size of the orifice, S_0 is the initial solder orifice size, n is the size scaling constant and d is the distance of the solder orifice from the stencil locus.

77. A system for designing a stencil for applying solder paste on a plurality of like electronic substrates, the system comprising:

a memory circuit;

a computer readable storage medium containing program instructions for execution by a processor; and

a processor connected to the memory circuit and the computer readable storage medium, the processor executing the program instructions stored on the computer readable medium to:

determining initial positions of a plurality of electrically conductive terminals in an initial terminal array to be carried by the substrates;

estimating a size scaling constant to reflect changes in positions of the terminals from their initial positions in light of anticipated handling of the substrates prior to solder deposition;

determining a stencil locus of the stencil;

arranging a plurality of solder orifices for the stencil, with a separate solder orifice corresponding to each terminal;

selecting an initial solder orifice size to deliver an appropriate volume of solder paste to an underlying terminal; and

sizing each solder orifice by multiplying the initial solder orifice size by a size scaling factor proportional to the size scaling constant, the size scaling factor being 1 at the stencil locus and changing outwardly therefrom in proportion to a distance of the orifice from the stencil locus.

78. The system of claim 77 wherein the size scaling constant is estimated by handling a plurality of electronic substrates similar to the substrates with which the stencil will be used according to the anticipated handling and measuring variations in positions of the terminals from their initial positions.

79. The system of claim 77 wherein the size scaling factor is estimated based on known behavior of the material of which the substrate is formed.

80. The system of claim 77 wherein a center of the stencil is identified as the stencil locus.

81. The system of claim 77 wherein the size of each orifice may be calculated according to the formula $S=S_0(1+nd)$, wherein S is the size of the orifice, S_0 is the initial solder orifice size, n is the size scaling constant and d is the distance of the solder orifice from the stencil locus.